IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: **David Shippy**	§	Group Art Unit: **2181**
	§	
Serial No. **10/821,025**	§	Examiner: **Meonske, Tonia L.**
	§	
Filed: **April 8, 2004**	§	Customer No. **50170**
	§	
For: **Architected Register File System Utilizes Status and Control Registers to Control Read/Write Operations Between Threads**	§	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

ATTENTION: Board of Patent Appeals and Interferences

APPELLANT'S REPLY BRIEF (37 C.F.R. 41.41)

This reply brief is in response to the Examiner's Answer mailed August 9, 2007.

No fees are believed to be required. If, however, any fees are required, I authorize the Commissioner to charge these fees which may be required to IBM Corporation Deposit Account No. 09-0447.

I. Response to Examiner's Remarks Regarding Rejection Under 35 U.S.C. 102

The Examiner's Answer states:

> It is noted that while there is no stated correspondence of threads to operand registers, it is explicitly stated in Sollars (column 3, lines 45-57 and column 15, lines 57-67) and acknowledged by the Appellant that there is a correspondence of threads to the control registers (See page 8 of the Appeal Brief).

Appellant notes that the rejection based on *Sollars* relies heavily on the Examiner's interpretation of the reference in this case. The Examiner has made several interpretations of the reference to establish a *prima facie* case of anticipation. If these interpretations are incorrect, or if the interpretations still fail to account for every claim feature, then, simply put, the reference fails to anticipate the claims.

In this case, the Examiner interprets the control register sets in the control register file in *Sollars* to be equivalent to the plurality of status and control registers recited in claim 1. The Examiner repeatedly points to sections of *Sollars*, such as those above, where *Sollars* appears to teach that one thread is given a privilege that allows the thread to access and modify the **status and control registers** of another thread. However, claim 1 does not recite one thread modifying the **status and control registers** of another thread.

Further to the above, the Examiner interprets the operand register files of *Sollars* to be equivalent to the plurality of register files recited in claim 1. However, *Sollars* simply fails to teach or fairly suggest allowing one thread to utilize an **operand register file** associated with another thread. The Examiner cannot interpret *Sollars* one way to teach one feature in the claim and then interpret *Sollars* the opposite way to teach another feature in the same claim. That is, the Examiner cannot interpret the control register sets in the control register file in *Sollars* to be equivalent to the plurality of status and control registers recited in claim 1 and interpret the operand register files of *Sollars* to be equivalent to the claimed register files, and then interpret the status and control register sets in the control register file in *Sollars* to be equivalent to the plurality of register files recited in claim 1. The interpretations must be consistent. The Examiner cannot mix and match interpretations to meet different features of the same claim.

The Examiner's Answer further states:

> It is also stated by Sollars in column 5, lines 7-19 that figure 1 shows all elements are coupled to each other. Upon inspection of figure 1, it can be seen that the

> control registers and the operand registers are coupled to each other. This coupling is a form of correspondence. Although there does not exist a direct correspondence, an indirect correspondence does exist and therefore meets the limitations of the claims. Therefore the examiner's rejection should be affirmed.

Appellant agrees that there appears to be a correspondence between the control register file and the operand register file. However, the Examiner does not show that *Sollars* teaches that each operand register file corresponds to a **respective thread**. The Examiner fails to establish how a control register file being coupled to an operand register file somehow results in a correspondence between a register file and a **thread**.

The Examiner's Answer states:

> It is also noted that there is no explicit limitation in claim 1 that recites that there is a control bit for the operand registers. The explicit limitation reads "each control bit set is at least configured to allow a thread associated with an associated SCR to utilize other register files associated with other threads." The term "other register files" is ambiguous and is interpreted to read "other SCR register files," and not interpreted as "other operand register files" as argued by Appellant.

As stated above, the rejection based on *Sollars* relies heavily on the Examiner's interpretation of the reference in this case. It is clear that claim 1 recites a plurality of register files. Throughout prosecution, the Examiner interpreted the operand register files of *Sollars* to be equivalent to the plurality of register files. Clearly, claim 1, for example, does not refer to the status and control register sets as register files. The only reasoning for the Examiner to shift interpretations of the reference, and now the claims, so late in the prosecution of this case is to warp the teachings of *Sollars* to somehow arrive at the claimed invention and to warp the claim language to better fit the teachings of *Sollars*. However Appellant disagrees that interpreting "other register files" to mean "other SCR register files" is a reasonable interpretation, because claim 1, for example, does not refer to the status and control register sets as "register files." Clearly, the recited "other register files" refers to the previously recited "plurality of register files." The Examiner cannot mix and match interpretations of the claim language to fit different teachings of the reference.

With respect to claims 16 and 19, the Examiner's Answer states:

> The claimed register files may be interpreted to be any type of register files, including the control register files.

While this may be true, the interpretations **must be consistent**. If the Examiner interprets the claimed register files to be control register files, then what of the status and control register sets? Simply stated, the Examiner cannot have it both ways. If the Examiner wishes to interpret the

claimed register files to be control register files, then *Sollars* clearly fails to teach the claimed status and control register sets. Furthermore, if the Examiner interprets the claimed register files to be control register files, then *Sollars* clearly fails to teach performing **the operation** where **the operation** is decoded from an **instruction** having an operations code field, a write field, and one or more read fields, wherein the operations code field defines a desired operation for the instruction, wherein the write field defines an address location to which a result of the operation is to be stored, and wherein the at least one read field defines an address location from which data is to be read for the operation, as recited in claims 16 and 19. Clearly such an operation would only read from or write to an operand register file, which defies the Examiner's interpretation.

With respect to claims 17 and 18, the Examiner's Answer argues that *Sollars* teaches thread manipulations at column 15, lines 60-66, which states:

> FIG. 20 illustrates the presently preferred embodiment of this context and thread based privilege approach. Each thread is initially conferred a standard thread privilege, which allows the thread to access and modify its own thread level control register set 106. On an as needed basis, one of the threads of each context is temporarily conferred a context privilege, which further allows the context privileged thread to access and modify the thread's context level control register set 104 as well as the peer threads' control register sets 106.

This cited portion merely teaches that a thread may modify a peer thread's control register sets. The Examiner's Answer states:

> Accessing a thread is done by reading a thread at a specified address from a read field of an instruction. Modifying a thread is writing to a thread at a specified register address indicated by a write field in an instruction.

Appellant respectfully disagrees. The Examiner is clearly filling in for the deficiencies of the references with the Examiner's own creation. *Sollars* makes no mention whatsoever of modifying a specified register address indicated by a write field in an instruction where a thread modifies a register in an operand register file associated with a different thread. In that sense, claims 17 and 18 recite something that is "different" from the teachings of *Sollars* because *Sollars* simply does not contemplate the claimed invention.

II. Response to Examiner's Remarks Regarding Rejection Under 35 U.S.C. 103

The Examiner's Answer states:

> However, Sollars has not only suggested, but has in fact explicitly taught a bit doublet in a status and control register (see Sollars, Fig. 9A, elements "sl" and "ll" comprise the bit doublet, also see Col. 10, lines 51-57) for separately enabling, or allowing, a thread to write to a register file associated with a different thread when the sl value is set to indicate that writing (or storing) is allowed (or not locked).).

Appellant respectfully disagrees. Col. 10, lines 51-57, of *Sollars* states:

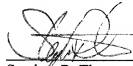
> Additionally, TCTL control register 112c comprises an sl value denoting whether the destination cache line of a store operation is to be locked, an sc value denoting whether the store data of a store operation is cacheable, and an sb value denoting whether store operations are to be forced to complete in program order.

The cited portion above appears to teach that the sl value denotes whether the destination **cache line** of a store operation is to be locked. *Sollars* does not teach that the sl value is used to denote whether a thread is allowed to write to a **register file associated with a different thread**. Therefore, the modification proposed by the Examiner must be based on hindsight reasoning and would not even result in the claimed invention.

III. Conclusion

In view of the above, Appellant respectfully submits that claims 1-9 and 16-21 of the present application are directed to statutory subject matter and that the features of these claims are not taught or suggested by the applied references. Accordingly, Appellant requests that the Board of Patent Appeals and Interferences overturn the rejections set forth in the Final Office Action.

Respectfully submitted,



Stephen R. Tkacs
Reg. No. 46,430
Walder Intellectual Property Law, P.C.
P.O. Box 832745
Richardson, TX 75083
(214) 722-6422
AGENT FOR APPELLANT